Kenneth Lin

(669) 261-0304 linkenneth6@gmail.com https://www.linkedin.com/in/linkeneth/

Summary

Computer Engineering Master's student with experience in flow automation and high-speed circuit characterization. Strong in clear and effective communication, with a growing interest in roles that bridge signal integrity and digital implementations for high-speed connectivity solutions.

Education

University of Southern California **2025 – Present**
Master's of Science in Computer Engineering *Los Angeles, California*
Relevant Coursework: VLSI System Design, Digital Signal Processing, Intergrated Memories

University of Massachusetts Amherst **2021 – 2025**
Bachelor of Science in Computer Engineering *Amherst, Massachusetts*
Relevant Coursework: VLSI Design, FPGA Security, Computer Architecture, Embedded Systems, Machine Learning

Experiences

Credo Semiconductor **June 2025 – Present**
Technology Design Co-Optimization Engineer intern *San Jose, CA*
- Delivered testbenches to characterize high-speed circuits across frequency, timing, and power metrics.
- Optimized Rx signal chain(CTLE, Sample & Hold, ADC) with ASO.ai to enhance signal integrity and performance.
- Migrating legacy Fusion Compiler flow to advanced PDK, reading RTL designs and compiling NDMs with Tcl.
- Developed MATLAB–PrimeWave pipeline for automated waveform post-processing, accelerating schematic validation.

University of Massachusetts Amherst **Sept 2024 – Dec 2024**
Undergraduate Instructional Assistant *Amherst, MA*
- Hosted biweekly office hours, supporting 120 students on FPGA security labs, quizzes, and homework.
- Led lab exercises, implementing circuits on FPGAs and integrating with Nios II processor in Quartus Prime.
- Facilitated student–professor communication to resolve issues and ensure smooth course delivery.
- Graded labs, homework, and exams, providing detailed feedback to students and instructor.

Credo Semiconductor **May 2024 – Aug 2024**
Foundry Engineer Intern *San Jose, California*
- Simulated PAM4 channels in MATLAB with FFE/DFE equalization, analyzing eye openings and ADC slicer offset.
- Reduced PLL simulation times by 400% on Synopsys CC through Verilog-A scripting and Simulink co-simulation.
- Migrated SerDes designs from Cadence Virtuoso to Synopsys CC, translating Tcl automation scripts to Perl.
- Coordinated with Synopsys and MathWorks application engineers on co-simulation workflows and tool integration.

Emerging Embedded Technologies Lab **Sep 2023 – Dec 2023**
Assistant Researcher *Amherst, Massachusetts*
- Researching capabilities of capturing Mixed Reality(MR) headset sensor data.
- Deployed MRTK, Photon Unity Networking, and MS Azure Spatial Anchors to create a collaborative MR environment.
- Scripted a C# program to capture headset data and relevant metrics into a CSV file for further analysis.
- Explored methods that adversaries could identify users based off of sensor readings.

Projects

PAM4 DSP Equalizer with 3-tap FFE / 1-tap DFE | *MATLAB, Verilog, Yosys/OpenROAD* **Summer 2026**
- Designed a SS-LMS adaptive 3-tap FFE/1-tap DFE, closing timing at 50MHz post-layout on SkyWater 130nm.
- Verified RTL via MATLAB co-sim, validated with eye-diagram metrics and BER analysis.
- Automated RTL-to-GDSII via Yosys and OpenROAD P&R, achieving DRC-clean, timing-clean signoff.

512-bit SRAM Array Design | *Cadence Virtuoso* **Spring 2026**
- Designed 512-bit SRAM array with peripheral logic, reaching 1GHz presim and 650MHz post-layout performance.
- Implemented SKILL script to automate hierarchical layout generation, minimizing area through custom cell abutment.
- Rigorous verification through DRC/LVS sign-off, validating read/write operations with test vector sequences.

Technical Skills

Languages: MATLAB, Tcl, Bash, SystemVerilog, Python
Developer Tools: Android Studio, Adobe XD, Git, Quartus Prime
EDA Tools: Simulink, Synopsys(Design Compiler, CC, HSPICE, FC), Cadence(Virtuoso, Pegasus, Innovus), ModelSim
Other technologies: MS Office, JMP, Unity, Wireshark, RHEL8, TensorFlow

Leadership / Extracurricular

Culinary Arts Club **2022 – 2025**
Vice President, Co-founder *University*
- Coordinate and host weekly cooking sessions, directing a team of 20 members in an industrial grade kitchen.
- Scripted a Discord bot synced to Jira cloud to automate task handling, pushing tasks with approaching deadlines.
- Strategically mapped out a term budget of $17,000 to fund club events, ensuring efficient resource allocation.